PM7351

S/UNI™ VORTEX

S/UNI-VORTEX

OCTAL SERIAL LINK MULTIPLEXER

DEVICE ERRATA

RELEASED

ISSUE 4: JUNE 2000

REVISION HISTORY

Issue No.	Issue Date	ECN	Details of Change
Issue 4	June, 2000	2594	Updated errata for production release. Updated functional discrepancies. Removed items pertaining to prototype devices or preliminary data sheet only.
Issue 3	January, 2000	N/A	Added revised text for LVDS signal amplitude. Added revised text for CELLXFERRI interrupt description. Removed Revision A functional discrepancies resolved in Rev B.
Issue 2	December, 1999	N/A	Updated receive timing reference jitter specification. Listed Revision B fixes to Revision A functional discrepancies.
Issue 1	July ,1999	N/A	

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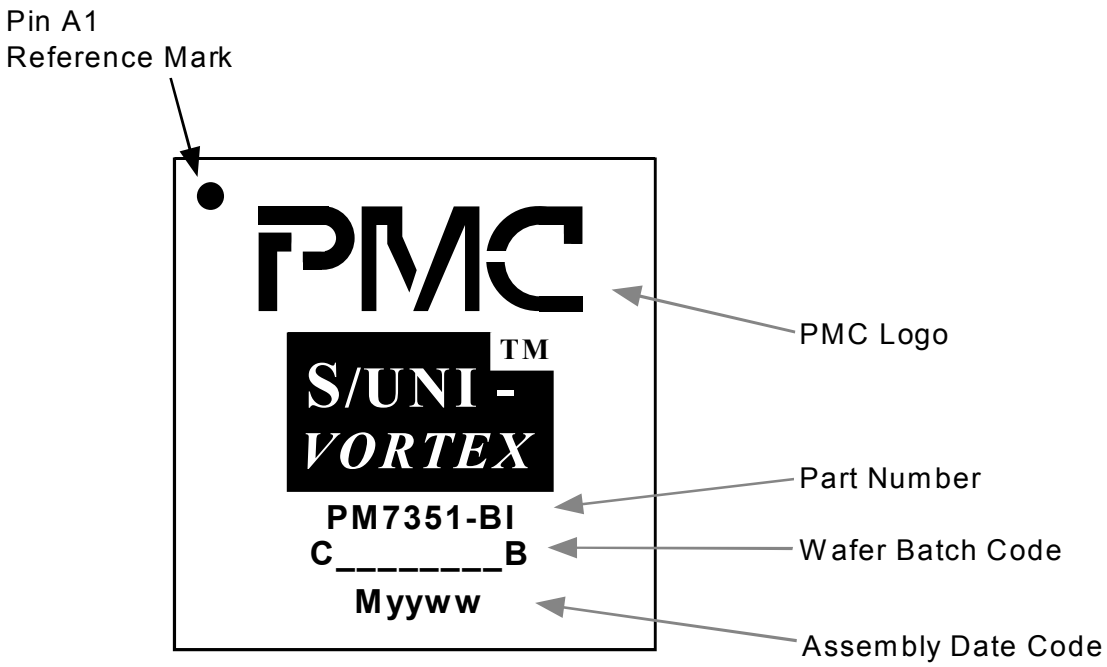
1 INTRODUCTION

The information contained in this document applies to Revision B of PM7351 S/UNI-VORTEX only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device (as shown in Figure 1).

Figure 1 – Device Marking



SCALE = 2:1 (Approx.)

The information contained in this document applies to Issue 5 of the PM7351 S/UNI-VORTEX Data Sheet only.

Reference:

PMC-980582, PM7351 S/UNI-VORTEX Octal Serial Link Multiplexer Data Sheet, Issue 5, March, 2000.

2 FUNCTIONAL DEFICIENCIES

This section lists the known functional deficiencies of the S/UNI-VORTEX device as of the publication date of this document. For each deficiency, the known work-around and operating constraints, if any, are described.

Please report any functional deficiencies observed to PMC-Sierra at:

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2.1 Anomalous TPA Behavior Following Bus Violation

Document References

S/UNI-VORTEX Octal Serial Link Multiplexer Data Sheet, Sections 9, 12, and 13.

Description

In very limited circumstances, the S/UNI-VORTEX may enter a state where the device will not assert the TPA output signal correctly. The symptom of this problem is that once a cell has been transferred downstream to a given logical channel, the TPA output for that channel will not be asserted until the TSX input is asserted (i.e. a new cell is transferred to *any other* logical channel on the entire bus). This can prevent the sequential transfer of cells to a single logical channel on the affected device. When using the S/UNI-APEX, any sequential cells that cannot be sent to a single channel will be sent during the next available opportunity following a cell transfer to another logical channel. This behavior will persist until the device is reset.

The S/UNI-VORTEX will enter this state only if the downstream bus protocol has been violated as indicated by the CELLXFERRI bit of the Downstream Cell Interface Interrupt Status register.

Resolution

Bus violations should never occur in normal operation except in cases of severe electrical interference. It is important to ensure that the hardware design and software programming do not inadvertently induce bus violations. Properly observing power-up and initialization sequences and using the appropriate PMC-Sierra device drivers will prevent any potential problems.

If a device *other than* the S/UNI-APEX is being used as bus master, the following measures should be observed to help prevent bus violations:

- The bus master should not attempt to write a cell to the S/UNI-VORTEX before the device is properly initialized. This can induce a bus violation when the bus master attempts to write a cell longer or shorter than expected by the S/UNI-VORTEX (If not explicitly set, this default is 56 bytes). The device should be properly initialized as described in *S/UNI-VORTEX Octal Serial Link Multiplexer Data Sheet*, Section 12.

- The bus master should not hold the TSX signal high while the S/UNI-VORTEX is in reset. For non-S/UNI-APEX devices, it may be necessary to use a pull-down resistor on this signal line to prevent a violation from occurring during initialization.

- The bus master should not violate the bus protocol during operation. Any attempts to transfer a cell that is longer or shorter than expected by the S/UNI-VORTEX or otherwise violate the bus protocol will set the CELLXFERRI bit of the Downstream Cell Interface Interrupt Status register which will reliably indicate that a violation has occurred.

Bus violations caused by severe electrical interference could also cause the CELLXFERRI bit to be set. Because the S/UNI-VORTEX will still continue to transfer cells even after a bus violation, a software reset of the device can be deferred indefinitely.

If the S/UNI-VORTEX enters this anomalous state, the only case where cell transfers could halt completely is when there is one, and *only* one, active downstream channel on any device on the entire loop bus. In this case, cells for this channel will queue indefinitely until a TSX signal is asserted on the bus. Again, the bus violation can be reliably detected via the CELLXFERRI bit and a software reset performed to clear the problem.

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